Memory devices include electrically erasable and electrically programmable read-only memories (EEPROMs) of flash electrically erasable and electrically programmable read-only memories (flash EEPROMs). Generally, flash EEPROM cells having both functions of electrical programming and erasing may be classified into two categories, namely, a stack-gate structure and a split-gate structure, which is not discussed here. A conventional stack-gate type cell is shown in Fig. 1 where,

On page 3, all of page 3, has been amended as follows:

as is well known, tunnel oxide film (20), a floating gate (30), an interpoly insulating film (40) and a control gate (50) are sequentially stacked on a silicon substrate (10) between a drain region (13) and a source region (15) separated by channel region (17). Substrate (10) and channel region (17) are of a first conductivity type, and the first (13) and second (15) doped regions are of a second conductivity type that is opposite the first conductivity type.

The programming and erasing of the flash EEPROM shown in Fig. 1 is accomplished electrically and in-circuit by using Fowler-Nordheim (F-N) tunneling, as it is known in the art. Basically, a sufficiently high voltage is applied to control gate (50) and drain (13) while source (15) is grounded to create a flow of electrons in channel region (17) in substrate (10). Some of these electrons gain enough energy to transfer from the substrate to control gate (50) through thin gate oxide layer (20) by means of (F-N) tunneling. The tunneling is achieved by raising the voltage level on control gate (50) to a sufficiently high value of about 12 volts. As the electronic charge builds up on floating gate (30), the electric field is reduced, which reduces the electron flow. When, finally, the high voltage is removed, floating gate (30) remains charged to a value larger than

On page 4, all of page 4, has been amended as follows:

the threshold voltage of a logic high that would turn it on. Thus, even when a logic high is applied to the control gate, the EEPROM remains off. Since tunneling process is reversible, floating gate (30) can be erased by grounding control gate (50) and raising the drain voltage, thereby

causing the stored charge on the floating gate to flow back to the substrate. Of importance in the tunneling region is the quality and the thinness of the tunneling oxide separating the floating gate from the substrate.

The thicknesses of the various portions of the oxide layers on the stacked-gate flash memory cell of Fig. 1 play an important role in determining such parameters as current consumption, coupling ratio and the memory erase-write speed, especially in an environment where feature sizes in advanced integrated circuits are being scaled down at a rapid rate. In prior art, various methods have been developed to address these parameters. For example, EPROMs having a trench-like coupling capacitors have been disclosed to address the shrinking area of the gate electrodes, and hence the capacitive coupling ratio between the floating gate and control gates on a conventional prior art EPROM.

In US Patent 5,480,821, Chang discloses a method of fabricating source-coupling, stacked-gate, virtual ground

On page 14, 2nd paragraph has been amended as follows:

The active regions are next defined with a photolithographic step and field regions grown, as is well known in the art. A photoresist pattern is normally used to protect all areas on which active devices will later be formed. The nitride layer is then dry etched, and the pad oxide may be etched by means of either a dry-or wet-chemical process. The etching is further carried into the substrate to form the shallow trench (130) that is shown in Fig. 2b. The photoresist layer is next removed by oxygen plasma ashing and then the inside walls of trench (130) is lined with an oxide layer (140) by thermal growth. Subsequently, the trench is filled with isolation oxide (150), thus forming shallow trench isolation (STI) as shown in Fig. 2b. Next, the substrate is subjected to chemical-mechanical polishing (CMP) after which the nitride layer is removed. The removal of nitride layer can be accomplished in a high-density-plasma (HDP) etcher with etch recipe comprising gases O_2, SO_2, CF_4 and He at flow rates between about 10 to 250, 10 to 80, 0 to 50 sccm and 40 to 80 sccm, respectively. The pad oxide layer (110) underlying nitride layer (120) is also

On page 18, please amend the 1st paragraph as follows: